Docket No. 2016-1537

In the

United States Court of Appeals

For the

Federal Circuit

GOLDEN BRIDGE TECHNOLOGY, INC.,

Plaintiff-Appellant,

v.

APPLE INC.,

Defendant-Appellee.

Appeal from the United States District Court for the Northern District of California
Case No. 5:12-cv-04882-PSG · Judge Paul S. Grewal

BRIEF OF APPELLANT

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April 1, 2016

CERTIFICATE OF INTEREST

Counsel for plaintiff-appellant Golden Bridge Technology, Inc. certifies the following:

1. The full name of every party or *amicus* represented by me is:

   Golden Bridge Technology, Inc.

2. The name of the real party in interest represented by me is:

   Golden Bridge Technology, Inc.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or *amicus curiae* represented by me are:

   None.

4. The names of all law firms and the partners or associates that appeared for the party or *amicus* now represented by me in the trial or agency or are expected to appear in this court are:

   COMPUTERLAW GROUP LLP
   Giacomo A. Russo

   MCKOOL SMITH HENNIGAN, P.C.
   Lawrence Hadley
   Roderick Dorman.

Dated: April 1, 2016

COMPUTERLAW GROUP LLP

By: /s/ Jack Russo
Jack Russo

Attorneys for Plaintiff-Appellant
GOLDEN BRIDGE TECHNOLOGY, INC.

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STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, Plaintiff-Appellant provides:

(a) There have been no previous appeals in this case.

(b) Plaintiff-Appellant is not aware of any other case that will directly affect or be directly affected by the Court's decision in this appeal.

JURISDICTIONAL STATEMENT

This Court has jurisdiction under 28 U.S.C. § 1295(a)(1). The District Court did as well (28 U.S.C. §§ 1331) and the parties consented to the Magistrate Judge under 28 U.S.C. § 636(c) and Fed. R. Civ. P. 72(a). A final judgment was entered on May 4, 2015 and an award on costs on December 21, 2015. This appeal, limited to the latter, was timely noticed on January 20, 2016.

STATEMENT OF THE ISSUES

Whether this case *must* be remanded to the District Court for reevaluation of the cost award under a legal standard which allows for more than one "prevailing party" because Octane Fitness, LLC v. ICON Health & Fitness, Inc., 134 S. Ct. 1749 (2014) (hereinafter "Octane") effectively overruled Shum v. Intel Corp., 629 F.3d 1360 (Fed. Cir. 2010) (hereinafter "Shum")?

Alternatively, whether this case *should* be remanded to the District Court for reevaluation of the cost award under a legal standard which allows for more than one "prevailing party," because the Shum rule conflicts with most other Courts which hold that the District Judge is in the best position to evaluate if more than one party has prevailed?

STATEMENT OF THE CASE

I. PRELIMINARY STATEMENT.

Under Federal Rule of Civil Procedure 54(d)(1)[1], can there be only one prevailing party? In accord with Octane, most Federal Circuits leave that question for the sound discretion of the District Judge. This Circuit, in a split decision pre-Octane, rejects that approach and compels only one choice on District Judges. But Octane is now binding law and, as further explained below, it effectively overrules Shum.

In this patent infringement lawsuit, which was unsuccessfully countered by an assertion of invalidity, arguments consumed considerable resources during the litigation; neither was 100% successful. However, the Shum rule forced the District Court judge to choose one party to bear the costs of positions which both parties prevailed on: Apple won on its non-infringement defense but lost on its invalidity claim; GBT won on validity and lost on infringement. Both parties prevailed in certain respects; both parties failed in certain respects. Post-Octane, the Shum rule improperly disempowers the District Court from exercising its discretion; under Octane, the District Court clearly has greater discretion. That issue is now ripe for review. The Shum standard is an inflexible interpretation of a statute which is inherently flexible, and Octane requires that Shum be overruled.

[1] Rule 54 awards costs to prevailing parties.

Golden Bridge Technology, Inc. ("GBT") is a developer and licensor of wireless communications technology. GBT owns U.S. Patent Number 6,075,793 (the "'793 Patent") and sued Apple, Inc. ("Apple") for infringing that patent. Apple defended the suit by arguing the '793 Patent was invalid and not infringed; and after years of litigation, a jury determined that Apple was half right: the patent was not infringed but it was also not invalid.[2]

Apple was awarded $187,060.70 in costs under Rule 54(d)(1) despite the split verdict due to this Court's opinion in Shum, which GBT submits is an improperly rigid interpretation of the statutory requirement.

II. PROCEDURAL HISTORY.

GBT filed this infringement suit on May 8, 2012. (A00108). Apple responded by denying infringement, and asserting the '793 patent was invalid (A00179), before the case was ultimately transferred to the Northern District of California on September 11, 2012. (A00209). The case proceeded to trial beginning March 30, 2014 (A00220) and lasted two weeks. (A00272).
The Jury returned a verdict on June 16, 2014 ruling the '793 Patent was not invalid (as asserted by GBT) but not infringed (as asserted by Apple). (A00274).

[2] What this means for future revisions of Apple's iPhone line of products is an open question never considered by the District Court.

Apple then sought costs of $195,619.15 under Rule 54(d)(1) (A00278) to which GBT objected. (A00280). After a second round of requests (A00289) and objections (A00291), the Clerk awarded Apple $30,686.13. (A00294). Apple moved to review the order (A00105) and constrained by Shum, the District Court found Apple as the sole prevailing party and awarded $187,060.70 in costs. (A00001). Critically, the Order expressly relies on the Shum rule for the proposition that "there can only be one prevailing party within the meaning of Rule 54(d)." (A00003).

STATEMENT OF THE FACTS

GBT is a New Jersey corporation (A00228) and owner of numerous patents including the '793 Patent. (A00224). GBT has been an innovator in wireless technology for over twenty years, and developed a substantial portfolio of related U.S. and foreign patents. (A00228; A00234). The company was originally formed to build technology related to the then-proposed 3G wireless standard. (A00228). Once the 3G standard was established, GBT and its team of over 20 telecom and computer hardware engineers turned their focus towards extending and licensing the technology GBT had invented to multiple others in the industry. (A00232).

As part of those licensing efforts, GBT analyzed a number of Apple wireless products. Because GBT's licensing efforts were rebuffed by Apple, GBT filed suit against Apple in 2012. (A00108).

Apple's defense of invalidity consumed substantial resources at trial as it moved unsuccessfully for Summary Judgment, Judgment as a Matter of Law, and a Renewed Judgment as a Matter of Law. (A00067; A00086; A00100; A00104).

SUMMARY OF THE ARGUMENT

Is there just one "prevailing party" under Rule 54(d)(1) when a defendant successfully defends an infringement action and a plaintiff successfully prevails over an assertion of invalidity? Rule 54(d)(1) states in relevant part "costs . . . should be allowed to the prevailing party." But in complex litigation with many substantial issues on the table, the rule is ambiguous as it fails to address on *what* the party must prevail.

This Court has said a District Judge "must choose one, and only one, 'prevailing party.'" Shum, 629 F.3d at 1367 (emphasis added). However, most other Courts of Appeal have ruled otherwise; namely, that Rule 54(d)(1) means which party has prevailed on a claim, defense, or cross-claim. Therefore, in a complex case, there may be more than one "prevailing party" within the meaning of Rule 54.

The District Court recognized the issue but deferred to the majority (2-1) decision in Shum -- notwithstanding its binary approach endorsed by (if not now required by) Octane. In light of this ambiguity and the Supreme Court's

subsequent decision in Octane, it is now clear that the standard set forth in Shum is an overly rigid interpretation of the statutory guidelines and it must be overruled.

ARGUMENT

I. BECAUSE THE TEXT OF RULE 54(D)(1) IS AMBIGUOUS AND DOES NOT ADDRESS ON *WHAT* A PARTY MUST PREVAIL TO BECOME A "PREVAILING PARTY," DISTRICT JUDGES ARE IN THE BEST POSITION TO MAKE THESE DECISIONS.

This Court reviews this pure question of law *de novo*. Rule 54(d)(1) states, in relevant part, "costs . . . should be allowed to the prevailing party." These eight words raise at least as many issues which have been addressed in case law. Unfortunately, many of the cases mix these issues making the precedent imprecise, but the majority recognize the ambiguity and leave the matter to the District Judge's discretion.

A. Rule 54(d) is Ambiguous.

Rule 54(d)(1) is deceptively simple because the conclusion under any analysis is ultimately who pays and how much. There are, however, a number of different possibilities. Two issues often addressed are how much discretion does the word "should" allow, and what is the level of success necessary to be declared a "prevailing party"? Indeed, much of the substantial confusion around Rule 54(d)(1) involves these questions.

B. Given All The Relevant Factors, District Judges Must Exercise Discretion and Not Be Limited to an Artificially Binary Decision.

Here, the issue is on *what* exactly must a party prevail to be declared a "prevailing party". If a party must prevail on a case as a whole, then there necessarily may only be one "prevailing party". If a party must prevail on a claim, defense, or cross-claim then there may be, in complex cases, more than one "prevailing party". In some cases, there may be no prevailing party at all.[3]

II. THE FEDERAL CIRCUIT ADOPTED A RIGID "PREVAILING PARTY" ANALYSIS IN *SHUM* BASED ON AN INCORRECT LITERAL INTERPRETATION.

The Federal Circuit determined "there can only be one prevailing party" because "the plain language of Rule 54 unambiguously limits the number of prevailing parties in a given case to one because the operative term, 'prevailing party,' is singular." Shum, 629 F.3d at 1367 (emphasis added). This reasoning, dissected carefully, assumes the answer to singular "who" and "what" questions are equally singular: one party and "the case as a whole."[4]

[3] Currently, the rule set forth by the Federal Circuit in Shum holds that there may only be one "prevailing party" per case, however this is at odds with the Supreme Court's guidance in Octane and decisions in other Courts of Appeal as well.

[4] What happens in a patent action between competitors that results in findings for infringement of their patents and infringement on both sides? Or, of invalidity on both sides?

But other courts disagree and have apportioned costs according to who prevailed on each claim, defense, or cross-claim. This alternative application demonstrates the ambiguity in Rule 54(d)(1). Because the Supreme Court recently explained that the Federal Circuit must not "[superimpose] an inflexible framework onto statutory text that is inherently flexible", the Federal Circuit standard must change accordingly. Octane, 134 S. Ct. at 1756.

III. THE MORE FLEXIBLE STANDARD FOR "PREVAILING PARTY" ADOPTED BY MOST FEDERAL COURTS SHOULD APPLY IN THE FEDERAL CIRCUIT.

A. The Ninth Circuit Follows the Flexible Approach.

The Ninth Circuit has explained, "[i]n the event of a mixed judgment, however, it is within the discretion of a district court to require each party to bear its own costs." Amarel v. Connell, 102 F.3d 1494, 1523 (9th Cir. 1997).

Other Federal courts have also determined that a party may prevail on something less than the entire case to be considered a "prevailing party." Ninth Circuit courts follow this more flexible standard:

> Although Duffy prevailed on a small portion of his claims the bulk of the effort and costs in this litigation were [otherwise, thus]the Court determines that Duffy.. pay defendant's costs, and that Duffy's partial success is adequately reflected by awarding him his own reasonable requested costs…."

Andresen v. Int'l Paper Co., 2015 U.S. Dist. LEXIS 75912, at *13–14 (C.D. Cal. Jun. 10, 2015) (emphasis added).

B. Most Other Federal Circuit Courts Follow the Flexible Approach of the Ninth Circuit.

Other Federal Courts have come to the same conclusion. The Eighth Circuit explained: "when a defendant counterclaims for affirmative relief and neither party prevails on its claim, it is quite appropriate to deny costs to both parties." Kropp v. Ziebarth, 601 F.2d 1348, 1358 n.27 (8th Cir. 1979). The Seventh Circuit agrees: "considering the mixed outcome of the civil rights and malicious prosecution claims, the decision requiring each party to bear its own costs is within that discretion." Testa v. Vill. of Mundelein, 89 F.3d 443, 447 (7th Cir. 1996). The Second Circuit adheres to the same view: "In a case such as this where the defendant counter-claims for affirmative relief and neither party prevails on its claim, it is quite appropriate to deny costs to both parties[.] . . ." Srybnik v. Epstein, 230 F.2d 683, 686 (2d Cir. 1956). And the Sixth Circuit is in accord as well: "At best this can only be described as a close and difficult case. The District Judge did not abuse his discretion in requiring each party to pay its own costs." U.S. Plywood Corp. v. Gen. Plywood Corp., 370 F.2d 500, 508 (6th Cir. 1966) (emphasis added).

C. Most District Courts Also Use the Flexible Approach Under Rule 54.

Examples from District Courts are plentiful. "In November, 1994, a jury found that the Braun Patent was valid but not infringed and found for defendants on their patent misuse and equitable estoppel defenses." B. Braun Med., Inc. v. Abbott Labs., 38 F. Supp. 2d 393, 393 (E.D. Pa. 1999). "Exercising the discretion conferred upon me by Rule 54, I will vacate the Clerk's taxation and direct that each party is to bear its own costs." B. Braun Med., 38 F. Supp. 2d at 395.

Furthermore, a

> [d]efendant may continue to manufacture the accused snowplows; plaintiff has a judicial declaration of patent validity; neither was able to establish that the other was liable in damages. [¶] In this case, regardless of who is the prevailing party, if either, to deny costs to both parties does not, as a practical matter impose a penalty on either party. Rule 54(d) speaks in terms of a 'prevailing party.' In the context of this case, in practical effect, there was no prevailing party and no losing party. The litigation resulted in a tie. Neither is entitled to costs.

Compro-Frink Co. v. Valk Mfg. Co., 595 F. Supp. 302, 304 (E.D. Pa. 1982) (emphasis added).

IV. THE SUPREME COURT'S *OCTANE* RULING EFFECTIVELY OVERRULES THE FEDERAL CIRCUIT'S ARTIFICIALLY INFLEXIBLE RULE 54(D) STANDARD.

In Octane, the Supreme Court recently held that the Federal Circuit's guidelines for determining attorney's fees were overly restrictive. That ruling is directly applicable to the Federal Circuit's artificially restrictive Shum rule.

The precise issue in Octane was 35 U.S.C. § 285 which states "[t]he court in exceptional cases may award reasonable attorney fees to the prevailing party." The Supreme Court overturned this Court's decision in Brooks Furniture Mfg. v. Dutailier Int'l, Inc., 393 F.3d 1378 (Fed. Cir. 2005), which had held that fees were appropriate "only if both (1) the litigation is brought in subjective bad faith, and (2) the litigation is objectively baseless." Brooks Furniture, 393 F.3d at 1381. The Supreme Court stated this Court's interpretation of the term exceptional "superimposes an inflexible framework onto statutory text that is inherently flexible." Octane, 134 S. Ct. at 1756. The High Court referred to the standard in Brooks Furniture as a "rigid and mechanical formulation." Id. at 1754.

Here, the Shum rule requires a similarly restrictive legal standard for "prevailing party" under Rule 54(d)(1). The Federal Circuit's split (2-1) Shum opinion that "the plain language of Rule 54 unambiguously limits the number of prevailing parties in a given case to one because the operative term, 'prevailing party,' is singular" assumes Rule 54 requires a party to win the case rather than something less. Shum, 629 F.3d at 1367 (emphasis added). This is not so in all cases and most Federal Courts have so held. See p. 9, supra.

Not only does Shum's interpretation fabricate a heightened legal standard, that standard does not fit the overall flexibility granted to District Judges as confirmed by Octane. Indeed, Octane makes clear that discretion is granted to

District Judges and that discretion is inherent in Rule 54's use of "should" rather than "must" in its express language. Octane makes clear that Congress emphasizes discretion with the word "should", and this extends to Rule 54 District Judge discretion as well.

CONCLUSION

In sum, Federal District Judges are in the best position to, and post-Octane, must have the power to decide if one, both, or neither party may be awarded costs (and in what amounts and with what offsets) because one, both, or neither have prevailed on the entire case or prevailed on something less. The District Judge is in the best position to weigh the successes, the failures, and the overall equities at stake and post-Octane, the Shum rule improperly denies the District Court its statutorily appointed discretion.

Indeed, District Court discretion is particularly important in patent cases where costs awards are many times higher than in non-patent litigation, and often a result of a war of attrition by defendants. For example, the court awarded $1,130,320 of requested $4,030,669 in costs in Oracle Am., Inc. v. Google Inc., 2012 U.S. Dist. LEXIS 125237, at *13 (N.D. Cal. Sept. 4, 2012) and another granted $1,110,639.75 in Apple Inc. v. Samsung Elecs. Co., 2015 U.S. Dist. LEXIS 111276, at *121 (N.D. Cal. Aug. 20, 2015).

Appellant GBT respectfully requests this Court overrule the Shum rule and in accord with Octane, expressly allow District Courts their inherent discretion to determine the "prevailing party" under Rule 54(d)(1). Accordingly, the cost award should be vacated and this case should be remanded for further proceedings using an appropriately flexible standard fully compliant with the Octane approach.

Dated: April 1, 2016

Respectfully submitted,

COMPUTERLAW GROUP LLP

By: /s/ Jack Russo
Jack Russo

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GOLDEN BRIDGE TECHNOLOGY, INC.

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

GOLDEN BRIDGE TECHNOLOGY, INC.,

Plaintiff,

v.

APPLE INC.,

Defendant.

Case No. 5:12-cv-04882-PSG

ORDER GRANTING REVIEW OF TAXATION OF COSTS

(Re: Docket No. 622)

After every trial, there is cleanup work. As part of its post-trial housekeeping, Defendant Apple Inc. requests review of the Clerk's taxation of costs against Plaintiff Golden Bridge Technology, Inc. Apple's motion is GRANTED.

I.

After a nine-day trial in June 2014, the jury found that Apple had not infringed GBT's patent and awarded no damages to GBT, but also found that Apple had not proved its invalidity defense.[1] The court entered judgment in favor of Apple,[2] and Apple sought taxation of costs against GBT.[3] GBT objected to several of the costs[4] and Apple accordingly waived a portion of them.[5] But GBT objected again,[6] and the Clerk taxed $30,686.13 in costs as follows:

[1] *See* Docket No. 548 at 2-3.

[2] *See* Docket No. 609.

[3] *See* Docket No. 611.

[4] *See* Docket No. 612-4.

[5] *See* Docket Nos. 615, 616.

Fees for printed or electronically recorded transcripts necessarily obtained for use in the case.	$24,331.07
Fees for exemplification and the costs of making copies of any materials where the copies are necessarily obtained for use in the case.	$3,911.06
Witness fees	$2,444.00
Total	**$30,686.13**[7]

Apple now moves for review and seeks the following costs:

Category	Sub-category	Clerk's taxation	Total costs sought on review
Transcripts	Hearing & trial transcripts	$24,331.07	$22,251.35
	Deposition transcripts		$25,351.07
	Deposition video recordings		$13,763.25
	Subtotal	**$24,331.07**	**$61.365.67**

Category	Sub-category	Clerk's taxation	Total costs sought on review
Witness Fees	Witness Fees	$2,444.00	$2,444.00
	Subtotal	**$2,444.00**	**$2,444.00**

Category	Sub-category	Clerk's taxation	Total costs sought on review
Exemplification & copies	Trial exhibits & witness binders	$3,911.06	$60,997.90
	Trial graphics		$17,617.61
	Electronic discovery		$44,635.52
	Subtotal	**$3,911.06**	**$123,251.03**

TOTAL	**$30,686.13**	**$187,060.70**[8]

II.

This court has jurisdiction under 28 U.S.C. §§ 1331 and 1338. The parties further consented to the jurisdiction of the undersigned magistrate judge under 28 U.S.C. § 636(c) and

[6] *See* Docket No. 620.

[7] *See* Docket No. 621.

[8] *See* Docket No. 622 at 3.

Fed. R. Civ. P. 72(a).[9]

III.

The court may exercise its discretion to award costs to the prevailing party.[10] A party "prevails when actual relief on the merits of [its] claim materially alters the legal relationship between the parties,"[11] and there can only be one prevailing party within the meaning of Rule 54(d).[12] "Determination of the prevailing party is based on the relation of the litigation result to the overall objective of the litigation, and not on the count of the number of claims and defenses" on which each party succeeded.[13] In patent infringement cases, a party that establishes non-infringement and avoids liability may be the prevailing party even though it is unsuccessful on an invalidity defense.[14]

Whether the Clerk's taxation of costs was appropriate must be analyzed according to the law of the regional circuit.[15] In the Ninth Circuit, there is a "strong presumption" in favor of awarding costs to the prevailing party.[16] By contrast, the burden is on the non-prevailing party to show why taxable costs should not be awarded.[17] To deny such an award, the district court must

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[9] *See* Docket Nos. 256, 257.

[10] *See Manildra Mill Corp. v. Ogilvie Mills, Inc.*, 76 F.3d 1178, 1183 (Fed. Cir. 1996) ("As the Supreme Court noted in *Farrar*, even if a party satisfies the definition of prevailing party, the district court judge retains broad discretion as to how much to award, if anything.").

[11] *Manildra Mill Corp.*, 76 F.3d at 1182 (internal quotation marks omitted).

[12] *See Shum v. Intel Corp*, 629 F.3d 1360, 1367 (Fed. Cir. 2010).

[13] *Brooks Furniture Mfg., Inc. v. Dutailier Int'l, Inc.*, 393 F.3d 1378, 1381 (Fed. Cir. 2005) (abrogated on other grounds by *Octane Fitness, LLC v. ICON Health & Fitness, Inc.*, 134 S. Ct. 1749 (2014)).

[14] *See, e.g.*, *Brooks Furniture Mfg., Inc.*, 393 F.3d at 1381; *Kinzenbaw v. Case LLC*, Case No. 05-cv-01483, 2006 WL 1096683, at *3 (Fed. Cir. Apr. 26, 2006); *Emblaze Ltd. v. Apple Inc.*, Case No. 5:11-cv-01079-PSG, 2015 WL 1304779, at *3-4 (N.D. Cal. March 20, 2015).

[15] *See Manildra*, 76 F.3d at 1183 ("Even if a party satisfies the definition of prevailing party, the district court judge retains broad discretion as to how much to award, if anything.").

[16] *Apple Inc.*, 2014 WL 4745933, at*5 (citing *Miles v. California*, 320 F.3d 986, 988 (9th Cir. 2003)).

provide specific reasons identifying why a particular case is not ordinary and that special circumstances exist.[18] These circumstances are extremely limited.[19]

IV.

Applying the above standards, the court finds that Apple was the prevailing party and is entitled to its taxable costs. Although Apple did not invalidate GBT's patent, it succeeded in its non-infringement defense and achieved its overall litigation objective of avoiding liability.[20]

First, Apple requests costs for three categories of transcripts: hearing and trial transcripts, deposition transcripts and deposition video recordings.[21] Under 28 U.S.C. § 1920, a prevailing party may recover "[f]ees for printed or electronically recorded transcripts necessarily obtained for use in the case." The hearing transcripts were used for trial briefing and Apple's motions for judgment as a matter of law, and thus were necessarily incurred for use in this case.[22] As for the expedited and realtime costs for the trial transcripts,[23] although this court does not award these

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[17] *Id*.

[18] *Save Our Valley v. Sound Transit*, 335 F.3d 932, 945 (9th Cir. 2003); *Champion Produce, Inc. v. Rudy Robinson Co.*, 342 F.3d 1016, 1022 (9th Cir. 2003).

[19] *See Quan v. Computer Sciences Corp.*, 623 F.3d 870, 888-89 (9th Cir. 2010) (internal citation and quotation marks omitted); *Emblaze Ltd.*, 2015 WL 1304779 at *4 n.32.

While Emblaze may try to argue that—as a small company—it falls into the first category, this category typically covers indigent plaintiffs or low-income individuals or groups in civil rights cases who appropriately receive an exception under the Ninth Circuit standard. *See, e.g.*, *Assoc. of Mex.-Am. Educators v. State of Cal.*, 231 F.3d 572 (9th Cir. 2000); *Bowoto v. Chevron Corp.*, Case No. 99-cv-02506, 2009 WL 1081096 (N.D. Cal. Apr. 22, 2009); *Schaulis v. CTB/McGraw-Hill, Inc.*, 496 F. Supp. 666 (N.D. Cal. 1980). Under this precedent, Emblaze's "limited financial resources" in the context of a patent case simply do not appear to count.

[20] *See* Docket No. 548 at 2-3.

[21] *See* Docket No. 622 at 5-6.

[22] *See* Docket No. 622 at 5.

[23] *See id.*

types of costs as a matter of course,[24] the undersigned's experience with patent trials like the one in this case has been that expedited trial transcripts and real-time transcription are in fact "necessarily obtained." When trial judges push hard on parties at trial to raise objections and motions promptly—so as to minimize the burden on both judge and jury from delay—it is difficult to conclude otherwise.[25]

As for deposition transcripts and video recordings,[26] Section 1920 and Civ. L.R. 54-3(c)(1) allow the recovery of the cost, including video recording, of any deposition taken in connection with the case.[27] All of the deposed witnesses were named on the parties' trial witness lists and the majority testified as witnesses at trial.[28] Apple does not request any impermissible costs[29] associated with expediting or shipping the deposition transcripts.[30] Apple therefore shall receive its full requested transcript costs: $22,251.35 for hearing and trial transcripts, $25,351.07 for deposition transcripts and $13,763.25 for deposition video recordings.

Second, Apple requests exemplification and copy costs for its trial exhibits and witness binders, trial graphics and electronic discovery. Under 28 U.S.C. § 1920(4), "[f]ees for exemplification and the costs of making copies of any materials where the copies are necessarily

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[24] *See, e.g.*, *TransPerfect Global, Inc. v. MotionPoint Corp.*, Case No. 10-cv-02590, 2014 WL 1364792, at *4 (N.D. Cal. Apr. 4, 2014) (denying costs for trial transcripts delivered hourly and costs for RealTime); *Apple Inc.*, 2014 WL 4745933, at *7 (N.D. Cal. Sept. 19, 2014) (awarding only standard daily transcripts, but noting that Apple had withdrawn its costs request for expedited transcripts).

[25] *See Kinzenbaw*, 2006 WL 1096683, at *6. Because *Kinzenbaw* originated in the District of Iowa, the district court applied Eighth Circuit rather than Ninth Circuit law. But GBT offers no clear Ninth Circuit authority suggesting a different standard.

[26] *See* Docket No. 622 at 5-6.

[27] *See* 28 U.S.C. § 1920; Civ. L.R. 54-3(c)(1).

[28] *See* Docket Nos. 433, 436.

[29] *See Emblaze Ltd.*, 2015 WL 1304779 at *5.

[30] *See* Docket No. 622 at 6.

obtained for use in the case" are taxable. Civ. L.R. 54-3(d)(4)-(5) specify that "[t]he cost of reproducing trial exhibits is allowable to the extent that a Judge requires copies to be provided" and that "[t]he cost of preparing charts, diagrams, videotapes, and other visual aids to be used as exhibits is allowable if such exhibits are reasonably necessary to assist the jury or the Court in understanding the issues at trial." Apple's trial exhibit costs were incurred for presenting evidence at trial, including stamped exhibit copies and copies of the final set of admitted exhibits for both parties.[31] These costs are necessary and allowable.

As for the trial graphics and demonstratives, these also were "reasonably necessary"[32] because this case, like many patent cases, "is exactly the type of complex litigation that requires high-quality demonstratives for the edification of the jury."[33] Apple may recover costs associated with "the physical preparation and supplication of documents."[34] Moreover, these demonstratives did not present themselves, and so Apple also may recover the costs for the "in-court technician time and the equipment" necessary to present the demonstratives.[35]

As for electronic discovery, "only costs incurred specifically to produce documents to the opposing party are recoverable."[36] "[C]ourts in this district have approved a method that calculates what percentage of overall documents were produced to the opposing party and then applies that percentage to production-related costs in the vendor's invoices."[37] Hosting fees are excluded, however, because "the court does not tax hosting fees."[38] Apple seeks "physical

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[31] *See* Docket No. 622 at 7; Docket No. 616-2 at 5-8.

[32] Civ. L.R. 54-3(d)(5).

[33] *Id.* at *6.

[34] *Emblaze, Ltd.*, 2015 WL 1304779 at *7.

[35] *Id*. at *7.

[36] *Id.*

[37] *Id.*

[38] *Id.* (quoting *eBay Inc. v. Kelora Sys., LLC*, Case No. 10-cv-04947 et al., 2013 WL 1402736, at

preparation" costs directly relating to the electronic preparation, duplication and production of documents that it produced to GBT, and excludes the intellectual effort and hosting costs associated with this production.[39] It also seeks a percentage of its upload copy costs and work for load file preparations, which reflects the proportion of such costs that were associated with documents produced to GBT.[40] Because Apple seeks only costs incurred in producing documents to GBT, and excludes impermissible fees, it shall receive its full requested costs in this category.

In sum, in addition to the $30,686.13 previously taxed by the Clerk, Apple shall receive the following additional costs, for a total cost award of $187,060.70:

Category	Sub-category	Clerk's taxation	Costs awarded on review
Transcripts	Hearing & trial transcripts	$24,331.07	$22,251.35
	Deposition transcripts		$25,351.07
	Deposition video recordings		$13,763.25
	Subtotal	**$24,331.07**	**$61.365.67**

Category	Sub-category	Clerk's taxation	Costs awarded on review
Witness Fees	Witness Fees	$2,444.00	$2,444.00
	Subtotal	**$2,444.00**	**$2,444.00**

Category	Sub-category	Clerk's taxation	Costs awarded on review
Exemplification & copies	Trial exhibits & witness binders	$3,911.06	$60,997.90
	Trial graphics		$17,617.61
	Electronic discovery		$44,635.52
	Subtotal	**$3,911.06**	**$123,251.03**

TOTAL	**$30,686.13**	**$187,060.70**[41]

*17 (N.D. Cal. Apr. 5, 2013).

[39] *See* Docket No. 622 at 9.

[40] *See id.* at 9-10.

[41] *See* Docket No. 622 at 3.

SO ORDERED.

Dated: December 21, 2015

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
Northern District of California

US006075793A

United States Patent [19]

Schilling et al.

[11] Patent Number: 6,075,793

[45] Date of Patent: Jun. 13, 2000

[54] **HIGH EFFICIENCY SPREAD SPECTRUM SYSTEM AND METHOD**

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[73] Assignee: **Golden Bridge Technology, Inc.**, West Long Branch, N.J.

[21] Appl. No.: **09/020,105**

[22] Filed: **Feb. 6, 1998**

[51] **Int. Cl.**[7] **H04B 7/216**

[52] **U.S. Cl.** **370/441**; 370/335; 370/342; 375/200

[58] **Field of Search** 370/320, 335, 370/342, 349, 350, 441, 464, 477, 479; 375/200, 355, 356

[56] **References Cited**

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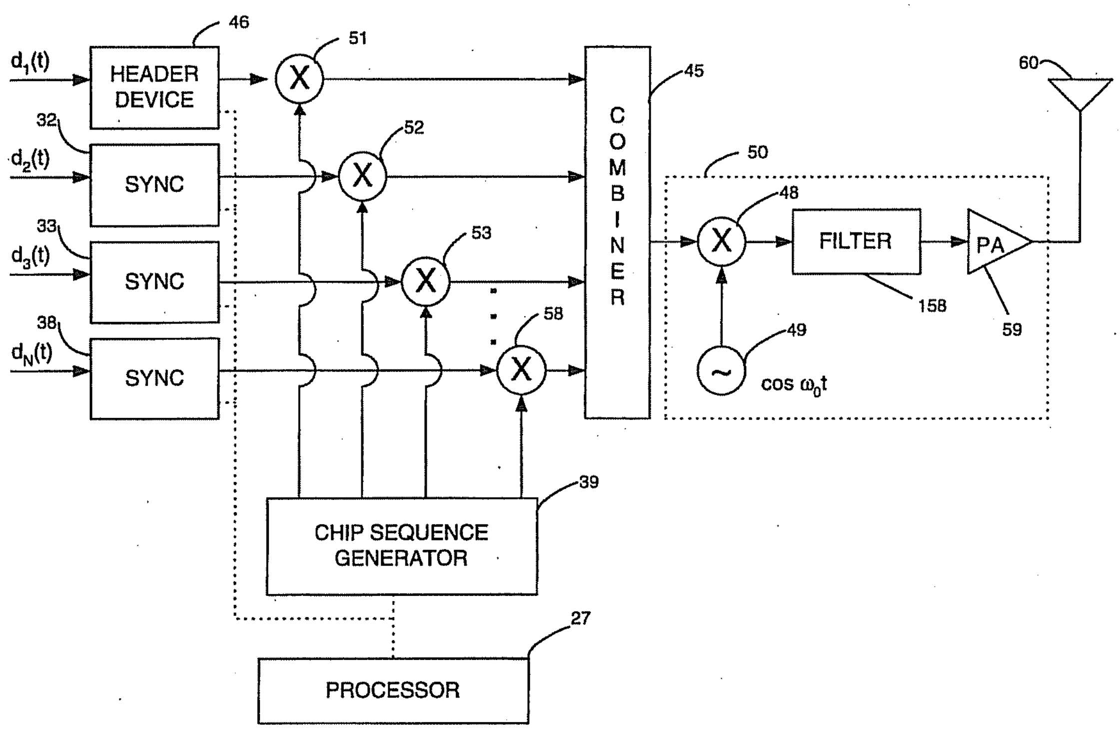
Primary Examiner—Dang Ton
Assistant Examiner—David R Vincent
Attorney, Agent, or Firm—David Newman; Chartered

[57] **ABSTRACT**

A multichannel-spread-spectrum system for communicating a plurality of data-sequence signals from a plurality of data channels using parallel chip-sequence signals in which fewer than all of the channels include header information. A header device concatenates a header to a first data-sequence signal on a first channel. Data-sequence signals in parallel channels are sent without a header, and are timed from the header in the first channel.

7 Claims, 4 Drawing Sheets



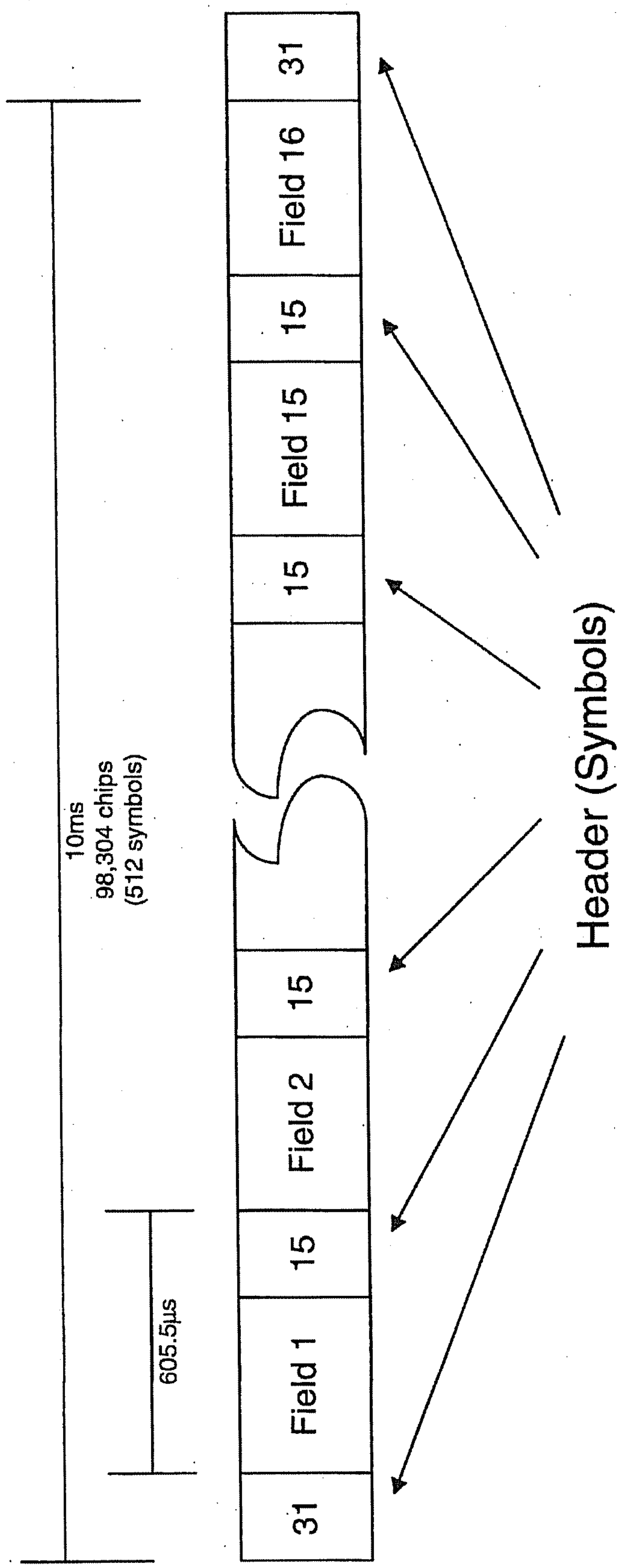


FIG. 1
PRIOR ART

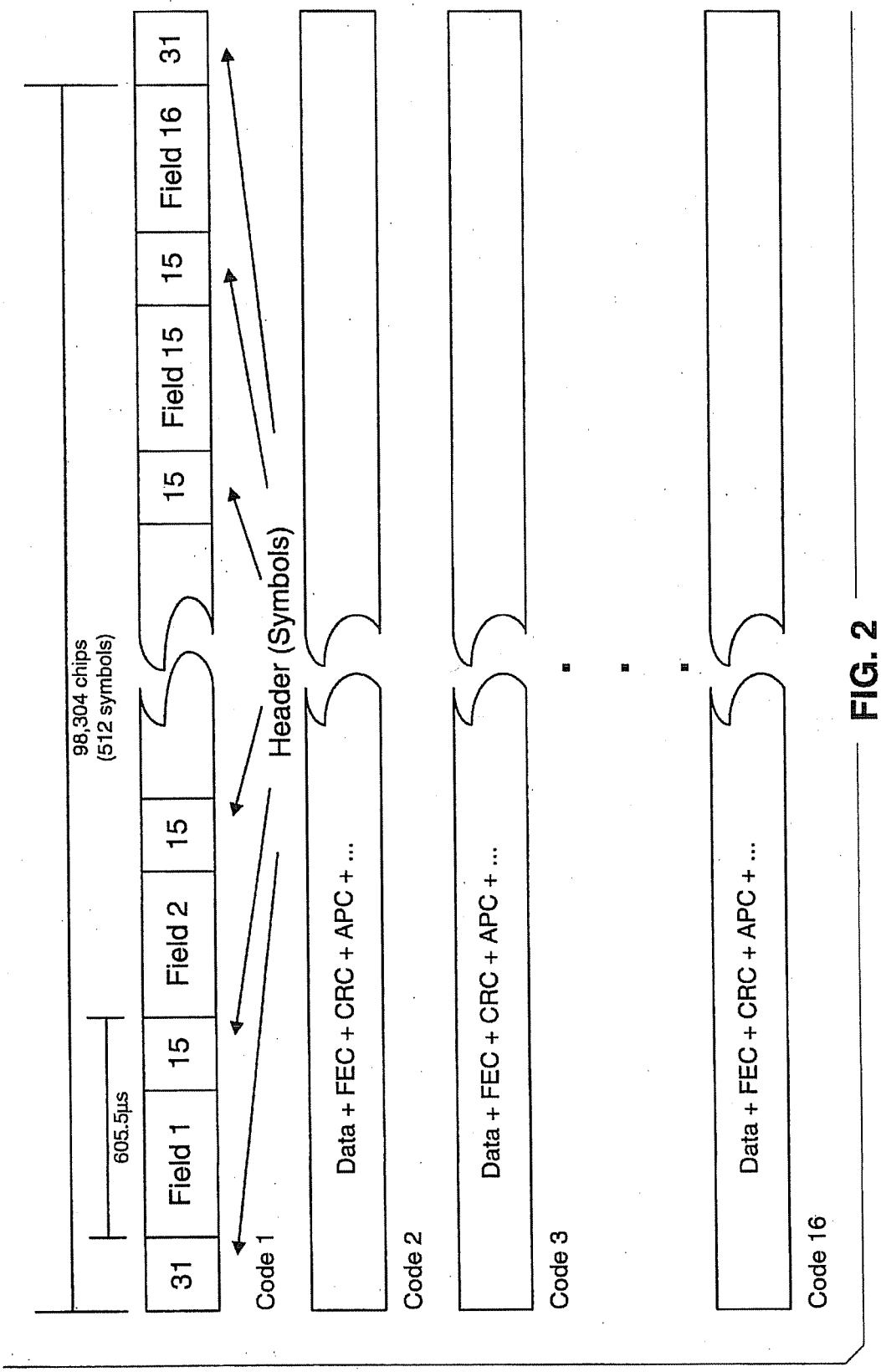

98,304 chips
(512 symbols)
605.5μs
31
Field 1
15
Field 2
15
15
Field 15
15
Field 16
31
Header (Symbols)
Code 1
Data + FEC + CRC + APC + ...
Code 2
Data + FEC + CRC + APC + ...
Code 3
Data + FEC + CRC + APC + ...
Code 16

FIG. 2

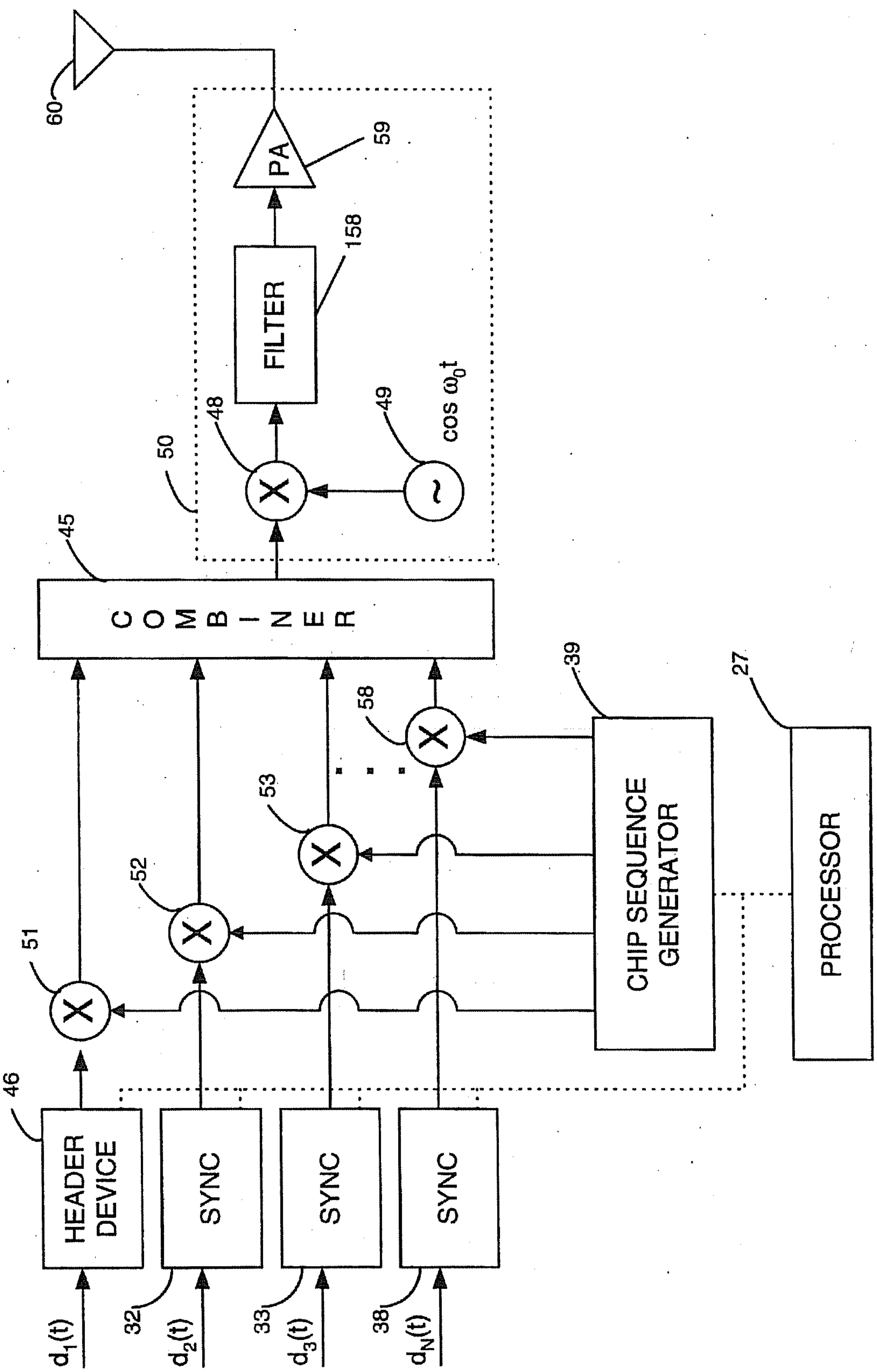

60
59
PA
158
FILTER
50
48
49
cos $\omega_0 t$
45
COMBINER
39
CHIP SEQUENCE GENERATOR
27
PROCESSOR
58
53
52
51
46
HEADER DEVICE
SYNC
SYNC
SYNC
32
33
38
$d_1(t)$
$d_2(t)$
$d_3(t)$
$d_N(t)$

FIG. 3

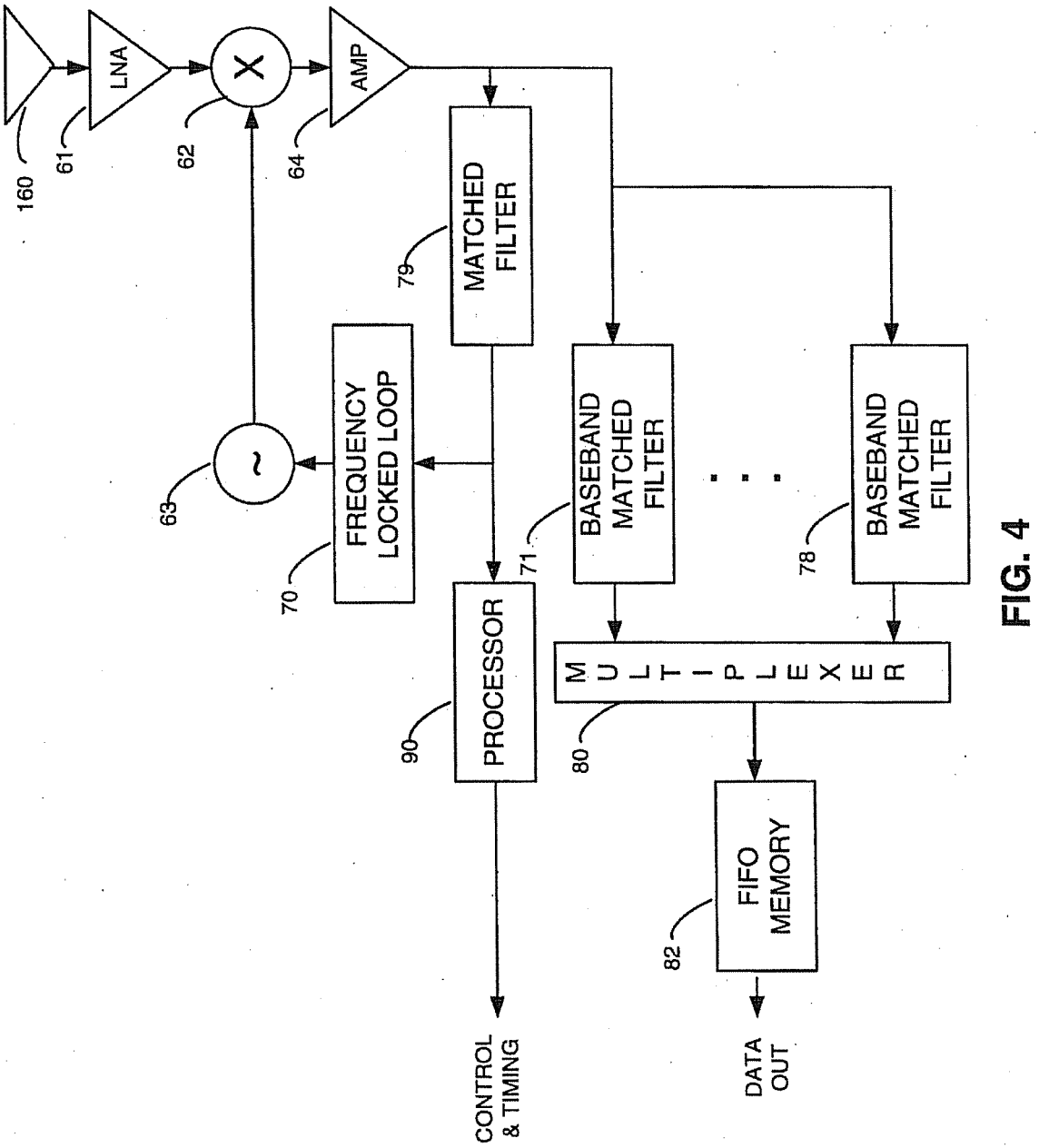

160
61
LNA
62
X
64
AMP
79
MATCHED FILTER
63
~
FREQUENCY LOCKED LOOP
70
71
BASEBAND MATCHED FILTER
78
BASEBAND MATCHED FILTER
90
PROCESSOR
MULTIPLEXER
80
82
FIFO MEMORY
CONTROL & TIMING
DATA OUT

FIG. 4

HIGH EFFICIENCY SPREAD SPECTRUM SYSTEM AND METHOD

BACKGROUND OF THE INVENTION

This invention relates to spread-spectrum communications, and more particularly to a highly efficient spread-spectrum system employing packets having multiple parallel spread-spectrum channels.

DESCRIPTION OF THE RELEVANT ART

In a spread-spectrum system, one method for constructing a spread-spectrum signal transmitted as a packet is to use a header to determine the sampling point of a matched filter, to time the fields of the received data, to determine the relative amplitudes of the in-phase component and quadrature-phase component of the received spread-spectrum signal for coherent detection, to detect multipath, and to provide the coefficients for maximal ratio combining. A typical frame of the spread-spectrum signal, transmitted as a packet or a frame of a continuous signal, is shown in FIG. **1** for the case where the processing gain (PG) is 192; that is, for the example where there are 192 chips/symbol. The term "packet" is used throughout this disclosure to indicate a packet signal, and also includes frames of continuous signals which define packets.

With reference to FIG. **1**, the time difference of 605.5 μsec between fields is needed when one or both of the terminals, transmitter and receiver, is in motion at vehicular speeds. Other times are also good. Less time between headers may be better in a particular application, but typically requires more headers, and hence more overhead. For the example of FIG. **1**, the Doppler shift of the received signal requires more frequent updates the faster one of the terminal moves. The example shown in FIG. **1** is for a system operating at 2 GHz, a vehicle at 60 miles per hour, and binary-phase-shift-keying (BPSK) modulation. The length of the headers, 31 and 15 symbols, is determined by the required signal-to-noise ratio of the headers to provide accurate enough references for coherent demodulation.

For the example of FIG. **1**, 256 symbols are used for headers, leaving 256 symbols for data. Thus, this channel is only 50% efficient. In addition, the maximum data rate, including bearer data, signaling, power control, etc., is 25.6 kbps uncoded.

One solution offered in the prior art is to use a lower processing gain, for example, 96. Then, there would be 1024 symbols per frame and the maximum data rate would increase to 51.2 kbps. The channel, however, would still be only 50% efficient. The headers would have to increase symbol length to make up for the loss in processing gain. Also, if orthogonal codes were used, then the number of users would be limited to 96.

Another method offered by prior art is to use parallel spread-spectrum channels, with each channel defined by a different chip-sequence signal. In this method, by using multiple correlators or matched filters, orthogonal codes are sent simultaneously, thereby increasing the data rate while still enjoying the advantage of a high processing gain. The multiple spread-spectrum channels merely behave as multiple users to a single location. However, the efficiency remains at 50%.

SUMMARY OF THE INVENTION

A general object of the invention is to increase data transmission efficiency by sending data through parallel spread-spectrum channels while including headers in fewer than all of the channels.

The present invention broadly includes a multichannel-spread-spectrum system for communicating a plurality of data-sequence signals from a plurality of data channels, over a communications channel. The multichannel-spread-spectrum system includes, at a transmitter, a header device, a processor, a chip-sequence generator, a plurality of product devices, a combiner, and a transmitter subsystem. At a receiver, the system may further include a translating device, a header-matched filter, a receiver processor, and a plurality of data-matched filters.

At the transmitter, the header device concatenates a header to a first data-sequence signal on the first data-sequence channel to generate a header frame. As used herein, a "header frame" is defined to be a header followed by data and may include multiple headers interspersed with fields of data. Timing is keyed from the header. The processor generates control and timing signals for synchronization of the second, third through the nth data-sequence channels to the header. The chip-sequence generator generates a plurality of chip-sequence signals, with each chip-sequence signal orthogonal to the other chip-sequence signals of the plurality of chip-sequence signals. A plurality of product devices multiplies the output from the header device, and each of the remaining data-sequence signals, by a respective chip-sequence signal, thereby generating a plurality of spread-spectrum channels. The plurality of spread-spectrum channels includes a spread-spectrum-header channel and a plurality of spread-spectrum-data channels. The spread-spectrum-header channel is generated by processing the header frame with a first chip-sequence signal. Each of the plurality of spread-spectrum-data channels is generated by processing a respective data-sequence signal by a respective chip-sequence signal. The combiner algebraically combines the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal. The transmitter subsystem transmits the multichannel-spread-spectrum signal on a carrier frequency using radio waves over the communications channel.

At the receiver, the translating device translates the received multichannel-spread-spectrum signal from the carrier frequency to a processing frequency. The header-matched filter has an impulse response matched to the header. The header-matched filter detects, at the processing frequency, the header in the multichannel-spread-spectrum signal and outputs, in response to detecting the header, a header-detection signal. The receiver processor, in response to the header-detection signal, generates control and timing signals. Each data-matched filter of the plurality of data-matched filters has an impulse response matched to a respective chip-sequence signal of the plurality of chip-sequence signals. The plurality of data-matched filters despreads the received multichannel-spread-spectrum signal as a plurality of received spread-spectrum channels.

Additional objects and advantages of the invention are set forth in part in the description which follows, and in part are obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention also may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate preferred

embodiments of the invention, and together with the description serve to explain the principles of the invention.

FIG. 1 illustrates a prior art packet or frame of a spread-spectrum signal;

FIG. 2 shows a spread-spectrum signal employing multiple parallel spread-spectrum channels, having a header for timing on only the first spread-spectrum channel;

FIG. 3 is a block diagram of a multichannel spread-spectrum transmitter; and

FIG. 4 is a block diagram of a multichannel spread-spectrum receiver.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference now is made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals indicate like elements throughout the several views.

The present invention provides a novel multichannel spread-spectrum system and method for communicating on a plurality of data channels using parallel spread-spectrum channels. With the present invention, increased efficiency is obtained by including header information in fewer than all the channels. Effectively, instead of replicating the frame format shown in FIG. 1 for each spread-spectrum channel, only one frame contains headers while the other spread-spectrum channels sent in parallel with different chip-sequence signals devote the entire time for data, as shown in FIG. 2. The remaining spread-spectrum channels are synchronized to the first channel by a processor. Therefore, the efficiency is increased. One or more spread-spectrum channels, but less than the total number of spread-spectrum channels, could have a header for synchronization. The use of one spread-spectrum channel with a header, however, would be more efficient. For example, a system constructed for 384 kbps data rate, FEC rate ½ convolutional coding, 25.6 kbps maintenance channel for power control, CRC, etc., and processing gain of 192, utilizes 16 parallel chip-sequence signals and yields a 96.9% efficiency.

The multichannel spread-spectrum system might be used as part of a radio-based Ethernet system, or an ATM system, or any other networked system. The multichannel spread-spectrum system could be used for connection as well as connectionless applications. The multichannel spread-spectrum system includes a multichannel spread-spectrum transmitter, and may also include a multichannel spread-spectrum receiver.

The present invention is for a multichannel spread-spectrum link which, in a preferred embodiment, is from a user to the base station. The present invention is illustrated, by way of example, with a multichannel spread-spectrum transmitter transmitting the multichannel spread-spectrum signal to a multichannel spread-spectrum receiver.

The multichannel spread-spectrum signal, in a preferred embodiment, includes a header, in a first data-sequence channel, followed in time by the first data-sequence signal. The header is concatenated with the first data-sequence signal to generate a header frame. As used herein, a "header frame" is defined to be a header followed by data and may include multiple headers interspersed with fields of data.

The header is generated from spread-spectrum processing, by using techniques well known in the art, a header-symbol-sequence signal with a chip-sequence signal. The header-symbol-sequence signal is a predefined sequence of symbols. The header-symbol-sequence signal may be a constant value, i.e., just a series of 1-bits or symbols, or a series of 0-bits or symbols, or alternating 1-bits and 0-bits or alternating symbols, a pseudorandom symbol sequence, or other predefined sequence as desired. The chip-sequence signal is user-defined and, in a usual practice, is used with a header-symbol-sequence signal. The header, in a preferred embodiment, includes a chip-sequence signal used for the purpose of synchronization.

Each spread-spectrum channel of the multichannel-spread-spectrum signal is generated similarly, from techniques well known in the art as used for the header, by spread-spectrum processing a data-sequence signal with a respective chip-sequence signal. The first chip-sequence signal is generated from a first code (code 1). A second spread-spectrum channel is defined by a second chip-sequence signal, which is generated from a second code (code 2). Similarly, a third spread-spectrum channel is defined by a third chip-sequence signal, which is generated from a third code (code 3).

The data-sequence signal may be derived from data, or an analog signal converted to data, signaling information, or other source of data symbols or bits. The chip-sequence signal can be user defined, and preferably is orthogonal to other chip-sequence signals used for generating the plurality of spread-spectrum channels. Demultiplexing data, spread-spectrum modulating each demultiplexed channel as a spread-spectrum signal and forming a multichannel spread-spectrum signal, keeps processing gain (PG) constant, independent of data rate. For a high data rate, for example, the multichannel spread-spectrum signal may include 128 channels. Sixty-four channels may be on an in-phase component and sixty-four channels may be on a quadrature-phase component.

The present invention broadly comprises a multichannel spread-spectrum system for communicating data between a plurality of multichannel spread-spectrum transmitters and a plurality of multichannel spread-spectrum receivers, preferably using radio waves. The terms "multichannel spread-spectrum transmitter" and "multichannel spread-spectrum receiver", as used herein, denote the overall system components for transmitting and receiving, respectively, data.

Each multichannel spread-spectrum transmitter includes header means, processor means, transmitter--spread-spectrum means, combiner means, and transmitter-carrier means. The header means is coupled to the processor means. The transmitter-spread-spectrum means is coupled to the header means and to a plurality of data channels. The combiner means is coupled between the transmitter-spread-spectrum means and the transmitter-carrier means.

The header means is coupled to a first channel of the plurality of data channels. The header means concatenates a header for chip-sequence synchronization to the first data-sequence signal of the plurality of data sequence signals to generate a header frame. The header is for chip-sequence synchronization.

The processor means is coupled to the header means and to each of remaining channels of the plurality of data channels. Responsive to the header, the processor means generates control and timing signals to synchronize the plurality of data channels to the header.

The transmitter-spread-spectrum means spread-spectrum processes each of the data-sequence signals, as well as the header frame, with a respective chip-sequence signal. The output of the transmitter-spread-spectrum means is a plurality of spread-spectrum channels, with each spread-spectrum

channel corresponding to one of the data inputs. The plurality of spread-spectrum channels includes a spread-spectrum-header channel and a plurality of spread-spectrum-data channels. The spread-spectrum channel is generated by processing the header frame with a first chip-sequence signal. Each of the plurality of spread-spectrum-data channels is generated by processing a respective data-sequence signal by a respective chip-sequence signal.

The combiner means algebraically combines the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal. At the output of the combiner means is the multichannel spread-spectrum signal. The transmitter-carrier means transmits, at a carrier frequency, the multichannel spread-spectrum signal, using radio waves, over a communications channel.

Each of the multichannel spread-spectrum receivers includes translating means, header-detection means, processor means, and receiver-spread-spectrum means. The translating means is coupled to the communications channel. The header-detection means is coupled between the translating means and the processor means. The receiver-spread-spectrum means is coupled to the translating means. At the output of the receiver-spread-spectrum means are the received data.

The translating means translates the received multichannel spread-spectrum signal from the carrier frequency to a processing frequency. The processing frequency may be a radio frequency (RF), an intermediate frequency (IF), a baseband frequency, or other desirable frequency for processing data.

The header-detection means detects, at the processing frequency, the header embedded in the spread-spectrum-header channel of the multichannel spread-spectrum signal. The header-detection means outputs, in response to detecting the header, a header-detection signal.

The receiver-processor means generates control and timing signals from the detected header. These signals are used for controlling sequences and timing of the invention.

The receiver-spread-spectrum means despreads the multichannel spread-spectrum signal of the multichannel spread-spectrum signal, as a plurality of data signals.

The transmitter-spread-spectrum means, as illustratively shown in FIG. **3**, is embodied as a chip-sequence means and a plurality of product devices **51–58**. The chip-sequence means may be embodied as a chip-sequence generator **39** for generating a plurality of chip-sequence signals. Alternatively, the transmitter-spread-spectrum means may be embodied as a plurality of EXCLUSIVE-OR gates, or equivalent logic devices or circuitry, coupled between the plurality of data inputs and a memory device for storing the plurality of chip-sequence signals. In this embodiment, the memory device outputs a respective chip-sequence signal to the respective data-sequence signal. A third alternative may include having the transmitter-spread-spectrum means embodied as a memory device, with appropriate detection circuitry so that, in response to a particular data symbol or data bit at the output of a particular output the demultiplexer, a chip-sequence signal is substituted for that data symbol or data bit. The transmitter-spread-spectrum means may also be embodied as any other technology known in the art capable of outputting a plurality of chip-sequence signals.

The combining means is embodied as a combiner **45**. The header means is embodied as a header device **46** for concatenating a header with data in the first data channel. The processor means is embodied as a processor **27**. The transmitter-carrier means is embodied as a transmitter-carrier subsystem **50**. The transmitter-carrier subsystem **50** may include an oscillator **49** and multiplier device **48** for shifting a signal to a carrier frequency, a filter **58** for filtering the shifted signal, and a power amplifier **59** and/or other circuitry as is well known in the art for transmitting a signal over a communications channel. The signal is transmitted using an antenna **60**.

As shown in FIG. **3**, the header device **46** is coupled between the first data channel and the first product device **51**. The chip-sequence generator **39** is coupled to the plurality of product devices **51–58** and to the processor **27**. The combiner **45** is coupled between the plurality of product devices **51–58** and the transmitter-carrier subsystem **50**.

The header device **46** concatenates the header with data using a first data channel of a plurality of data channels. The header device **46** is necessary for timing of data from different data channels. From timing the data from the header in a single channel, data in all channels are timed. A plurality of synchronization devices, which may be embodied as buffer memories **32–38**, receive timing and control signals from the processor **27** to synchronize the plurality of data channels to the header on the first data channel.

The chip-sequence generator **39** generates a plurality of chip-sequence signals. Each of the chip-sequence signals of the plurality of chip-sequence signals has low correlation with the other chip-sequence signals in the plurality of chip-sequence signals, and is preferably orthogonal to the other chip-sequence signals in the plurality of chip-sequence signals. The chip-sequence generator **39** equivalently may be embodied as a plurality of chip-sequence generators.

The plurality of product devices **51–58**, for example, may be embodied as a plurality of EXCLUSIVE-OR gates coupled between the incoming data channels and the chip-sequence generator **39**. Each EXCLUSIVE-OR gate multiplies a respective data-sequence signal by a respective chip-sequence signal from the chip-sequence generator **39**.

The plurality of product devices **51–58** multiplies each of the data-sequence signals by a respective chip-sequence signal. At the output of the plurality of product devices **51–58** is a plurality of spread-spectrum channels, respectively. A particular spread-spectrum channel is identified by the chip-sequence signal that was used to spread-spectrum process the particular data sequence signal. The plurality of spread-spectrum channels includes a spread-spectrum-header channel and a plurality of spread-spectrum-data channels. The spread-spectrum-header channel is generated by processing the header frame with a first chip-sequence signal. Each of the plurality of spread-spectrum-data channels is generated by processing a respective data-sequence signal with a respective chip-sequence signal. The plurality of spread-spectrum-data channels is synchronized to the spread-spectrum-header channel.

The combiner **45** algebraically combines the plurality of spread-spectrum channels, and outputs the combined signal as a multichannel-spread-spectrum signal. Preferably, the combiner **45** combines the plurality of spread-spectrum channels linearly, although some nonlinear process may be involved without significant degradation in system performance.

The transmitter-carrier subsystem **50** transmits, at a carrier frequency, the multichannel spread-spectrum signal using radio waves over a communications channel. The transmitter-carrier subsystem **50** of the multichannel spread-spectrum transmitter includes appropriate filters, power amplifiers and matching circuits coupled to an antenna **60**. The transmitter-carrier subsystem **50** also may include a

hard limiter, for hard limiting the multichannel spread-spectrum signal before transmitting.

At the receiver, as shown in FIG. **4**, the translating means is shown as receiver RF section, which may include a translating device **62** with oscillator **63** and frequency-locked loop **70**. The translating device **62** is coupled through a low noise amplifier **61** to an antenna **160** to the communications channel and through an amplifier **64** to the header-matched filter **79**. The translating device **62** is coupled to the oscillator **63**, and the oscillator **63** is coupled to the frequency-locked loop **70**. The header-matched filter **79** is coupled to the frequency-locked loop **70** and to a processor **90**. The plurality of data-matched filters **71–78** is coupled between the translating device **62** and a multiplexer **80**. The multiplexer **80** is coupled to a receiver-FIFO memory **82**.

The translating device **62** translates the received multichannel spread-spectrum-spread-spectrum signal from the carrier frequency to a processing frequency. The translating device **62** may be a mixer, which is well known in the art, for shifting an information signal, which in this disclosure is the received multichannel spread-spectrum signal modulated at a carrier frequency, to IF or baseband. The processing frequency may be RF, IF, baseband frequency or other desired frequency for a digital signal processor. The signal for shifting the received multichannel spread-spectrum-spread-spectrum signal is produced by oscillator **63**.

The header-detection means is embodied as a header-matched filter **79**. The header-matched filter **79** detects, at the processing frequency, the header embedded in the spread-spectrum-header channel of the multichannel spread-spectrum signal. The term "header-matched filter" as used herein, is a matched filter for detecting the header, by having an impulse response matched to the chip-sequence signal and bits of the header of the spread-spectrum-header channel of the multichannel spread-spectrum signal. The header-matched filter may be a digital-matched filter, a surface-acoustic-wave (SAW) device, software operating in a processor or embodied within an application specific integrated circuit (ASIC). In response to detecting the header, the header-matched filter **79** outputs a header-detection signal. The header-matched filter at a base station can detect the header embedded in the multichannel spread-spectrum signal from all users, since the chip-sequence signal for the header and data is common to all users.

The header-detection means alternatively may be embodied as a header-matched filter, coupled to an output of a data-matched filter or to the output of the multiplexer **80**. This alternative is taught in U.S. Pat. No. 5,627,855, entitled PROGRAMMABLE TWO-PART MATCHED FILTER FOR SPREAD SPECTRUM by Davidovici, which is incorporated herein by reference.

The frequency-locked loop **70** is frequency locked in response to the header-detection signal. The frequency-locked loop **70** locks the frequency of the oscillator **63** to the carrier frequency of the received multichannel spread-spectrum signal. Circuits for frequency locked loops, and their operation, are well known in the art.

The processor means is embodied as a processor **90**. The processor **90**, in response to the header-detection signal, generates control and timing signals. The control and timing signals are used for controlling sequences and timing of the invention.

The receiver-spread-spectrum means is embodied as a plurality of data-matched filters **71–78**. Each of the plurality of data-matched filters **71–78** has an impulse response matched to a chip-sequence signal of a respective one of the plurality of chip-sequence signals. The data-matched filters may be embodied as a digital-matched filter, SAW device, software operating in a processor, or an ASIC. The plurality of data-matched filters **71–78** despreads the multichannel-spread-spectrum signal as a plurality of received spread-spectrum channels.

Alternatively, the receiver-spread-spectrum means and the transmitter-spread-spectrum means may be embodied as the plurality of data-matched filters **71–78**, thereby using the same hardware. The plurality of data-matched filters **71–78** in this embodiment are time multiplexed with different coefficients, between transmit and receive.

Each chip-sequence signal in the plurality of chip-sequence signals is different, preferably orthogonal to the others, to avoid or reduce interference. The plurality of chip-sequence signals, however, preferably is common to all users. Thus, the plurality of data-matched filters **71–78** can detect the plurality of chip-sequence signals from any of the users.

The present invention also comprises a method. The method includes the steps of concatenating a header to a first data-sequence signal of a plurality of data sequence signals to generate a header frame. A used herein, a "header frame" is defined to be a header followed by data and may include multiple headers interspersed with fields of data.

The input data are in a plurality of data-sequence signals. The plurality of data-sequence signals are synchronized to the header responsive to control and timing signals generated by a processor. The method includes generating a plurality of chip-sequence signals, and multiplying each of the data-sequence signals by a respective chip-sequence signal, thereby generating a plurality of spread-spectrum channels. The plurality of spread-spectrum channels includes a spread-spectrum-header channel and a plurality of spread-spectrum-data channels. The spread-spectrum-header channel is generated by processing the header frame with a first chip-sequence signal. Each of the plurality of spread-spectrum-data channels is generated by processing a respective data-sequence signal with a respective chip-sequence signal. Each of the plurality of spread-spectrum-data channels is synchronized to the spread-spectrum-header channel.

The steps include algebraically combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal, and transmitting on a carrier frequency the multichannel spread-spectrum signal over a communications channel using radio waves.

The steps may further include, at a multichannel spread-spectrum receiver, translating the multichannel spread-spectrum signal from the carrier frequency to a processing frequency, and detecting, at the processing frequency, the header embedded in the multichannel spread-spectrum signal. The chip-sequence signals used for the header and the data may be common to all users. In response to detecting the header, the method includes outputting a header-detection signal and generating control and timing signals.

The steps also include despreading the multichannel-spread-spectrum signal as a plurality of received spread-spectrum channels.

In the present invention, assume 800 kb/s is first demultiplexed into K channels, where K=32 in a preferred system, although any K will suffice. As a result, if K=32, then the transmitted rate is f_T=25 kb/s. Each of these K channels is spread using a different orthogonal spread-spectrum code of length L. Thus,

$$\int_0^{T_L} C_i(t)C_j(t)\,dt = \begin{cases} 1 & i=j \\ 0 & i\neq j \end{cases}$$

over the time, T_L, corresponding to the code length L. For example, if the chip rate were 5 megachips/s, and there were eight users, then the send rate is 6.4 Mb/s 32=200 kb/s so that processing gain is 25.

Note that the processing gain has increased by a factor of 32. Further, the length L of each of the K orthogonal codes is such that L≧K, since there are only L orthogonal codes of length L.

One-half of the chip-sequence signals may be sent on an in-phase (I) channel and one-half on a quadrature-phase (Q) channel, forming quadrature-phase-shift-keying modulation (QPSK) or OQPAK. Binary-phase-shift-keying modulation (BPSK) can also be used. These are standard modulation procedures well known in the prior art.

Different sectors and different cells should use different orthogonal chip sequences to minimize interference between sectors and cells. This is done by multiplying each chip sequence signal, C_i, by a chip sequence, $g_d(t)$. Within a sector, every user uses the same codeset, C_i and g_j. Within each sector of each cell, each user uses the same codeset, C_i, but each sector in each cell gets a different g_j.

Users transmitting at different rates use a subset of the 32 codes so that the processing gain remains a constant.

If 2 Mb/s were the basic data rate, then with FEC and overhead the data rate might be f_d=4.4 Mb/s. In this case to achieve a processing gain of twenty-five (PG=25) at say f=10 Mchips/s requires:

$$25=Kf_c/f_d\times 8$$

or

$$K=200f_d/f_c=200\times 4.4/10=88$$

The use of 88 orthogonal codes each of length 88 is certainly within the state-of-the art.

It will be apparent to those skilled in the art that various modifications can be made to the high efficiency spread spectrum packet system of the instant invention without departing from the scope or spirit of the invention, and it is intended that the present invention cover modifications and variations of the high efficiency spread spectrum packet system provided they come within the scope of the appended claims and their equivalents.

We claim:

1. A multichannel-spread-spectrum system for communicating a plurality of data-sequence signals from a plurality of data channels using parallel chip-sequence signals, comprising:

a header device, coupled to a first data channel of said plurality of data channels, for concatenating a header to a first data-sequence signal;

a processor for synchronizing a remaining plurality of data channels to the header in the first data channel;

chip-sequence means for outputting a plurality of chip-sequence signals, with each chip-sequence signal orthogonal to the other chip-sequence signals in said plurality of chip-sequence signals;

a plurality of product devices, coupled to said chip-sequence means, for multiplying each of said plurality of data-sequence signals by a respective chip-sequence signal, thereby generating a plurality of spread-spectrum channels, respectively;

a combiner, coupled to the plurality of product devices, for algebraically combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal;

a transmitter subsystem, coupled to said combiner, for transmitting the multichannel-spread-spectrum signal on a carrier frequency over a communications channel;

a translating device, coupled to the communications channel, for translating the received multichannel-spread-spectrum signal from the carrier frequency to a processing frequency;

a header-matched filter, coupled to said translating device and having an impulse response matched to the header, for detecting, at the processing frequency, the header in the multichannel-spread-spectrum signal, and for outputting, responsive to detecting the header, a header-detection signal;

a receiver processor, coupled to said header-matched filter, responsive to the header-detection signal, for generating control and timing signals; and

a plurality of data-matched filters, coupled to said translating device, with each data-matched filter having an impulse response matched to a respective chip-sequence signal of the plurality of chip-sequence signals, for despreading the received multichannel-spread-spectrum signal as a plurality of received spread-spectrum channels, respectively.

2. The multichannel-spread-spectrum system as set forth in claim 1, with said chip-sequence means including a chip-sequence generator for generating the plurality of chip-sequence signals.

3. The multichannel-spread-spectrum system as set forth in claim 1, with said chip-sequence means including a memory for storing the plurality of chip-sequence signals.

4. The multichannel-spread-spectrum system as set forth in claim 1, said plurality of product devices including:

a first EXCLUSIVE-OR gate, coupled to said chip-sequence means and to said header device, for multiplying the header and a first data-sequence signal with a first chip-sequence signal to generate a spread-spectrum-header channel;

a second EXCLUSIVE-OR gate, coupled to said chip-sequence means and to a second data channel, for multiplying a second data-sequence signal by a second chip-sequence signal, the second chip-sequence signal being different from the first chip-sequence signal, to generate a first spread-spectrum-data channel;

a third EXCLUSIVE-OR gate, coupled to said chip-sequence means and to a third data channel, for multiplying a third data-sequence signal by a third chip-sequence signal, the third chip-sequence signal being different from the second chip-sequence signal and from the first chip-sequence signal, to generate a second spread-spectrum-data channel;

an nth EXCLUSIVE-OR gate, coupled to said chip sequence means and to an nth data channel, for multiplying an nth data-sequence signal by an nth chip-sequence signal, the nth chip-sequence signal being different from the third chip-sequence signal and from the second chip-sequence signal and from the first chip-sequence signal, to generate an nth–1 spread-spectrum-data channel; and

the first spread-spectrum-data channel, the second spread-spectrum-data channel, and the nth–1 spread-spectrum-data channel synchronized, responsive to timing and

control signals generated by the processor, to the spread-spectrum-header channel.

5. A multichannel-spread-spectrum transmitter for communicating a plurality of data-sequence signals from a plurality of data channels using parallel chip-sequence signals, comprising:

a header device, coupled to a first data channel of said plurality of data channels, for concatenating a header to a first data-sequence signal to generate a header frame;

a processor, coupled to the header device and to the plurality of data channels, for synchronizing the plurality of data channels;

spread-spectrum means, coupled to the plurality of data channels, for spread-spectrum processing the plurality of data-sequence signals by a plurality of chip-sequence signals, respectively, thereby generating a plurality of spread-spectrum channels, the plurality of spread-spectrum channels including a spread-spectrum-header channel generated by processing the header frame with a first chip-sequence signal, and a plurality of spread-spectrum-data channels;

combiner means, coupled to said spread-spectrum means, for algebraically combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal; and

carrier means, coupled to said combiner means, for transmitting the multichannel-spread-spectrum signal over a communications channel at a carrier frequency.

6. The transmitter as set forth in claim 5, said spread-spectrum means including:

means for generating the plurality of chip-sequence signals;

a first EXCLUSIVE-OR gate, coupled to said generating means and to said header device, for multiplying the header frame with the first chip-sequence signal to generate the spread-spectrum-header channel;

a second EXCLUSIVE-OR gate, coupled to said generating means and to a second data channel, for multiplying a second data-sequence signal by a second chip-sequence signal, the second chip-sequence signal being different from the first chip-sequence signal, to generate a first spread-spectrum-data channel;

a third EXCLUSIVE-OR gate, coupled to said generating means and to a third data channel, for multiplying a third data-sequence signal by a third chip-sequence signal, the third chip-sequence signal being different from the second chip-sequence signal and from the first chip-sequence signal, to generate a second spread-spectrum-data channel;

an nth EXCLUSIVE-OR gate, coupled to said generating means and to an nth data channel, for multiplying an nth data-sequence signal by an nth chip-sequence signal, the nth chip-sequence signal being different from the third chip-sequence signal and from the second chip-sequence signal and from the first chip-sequence signal, to generate an nth−1 spread-spectrum-data channel; and

the first spread-spectrum-data channel, the second spread-spectrum-data channel, and the nth−1 spread-spectrum-data channel synchronized, responsive to timing and control signals generated by the processor, to the spread-spectrum-header channel.

7. A multichannel-spread-spectrum transmitter for communicating a plurality of data-sequence signals from a plurality of data channels using parallel chip-sequence signals, comprising:

a header device, coupled to a first data channel of said plurality of data channels, for concatenating a header to a first data-sequence signal to generate a header frame;

a processor, coupled to the header device and to the plurality of data channels, for synchronizing the plurality of data channels;

a chip-sequence generator for generating a plurality of chip-sequence signals, each of said plurality of chip-sequence signals being orthogonal to other chip-sequence signals within the plurality of chip-sequence signals;

a plurality of product devices, coupled to the plurality of data channels and to said chip-sequence generator, for multiplying the plurality of data-sequence signals by a plurality of chip-sequence signals, respectively, thereby generating a plurality of spread-spectrum channels, the plurality of spread-spectrum channels including a spread-spectrum-header channel and a plurality of spread-spectrum-data channels, the spread-spectrum-header channel generated by multiplying the header frame with a first chip-sequence signal, each of the plurality of spread-spectrum-data channels generated by multiplying a respective data-sequence signal by a respective chip-sequence signal;

a combiner, coupled to said plurality of product devices, for algebraically combining the plurality of spread-spectrum channels as a multichannel-spread-spectrum signal; and

a transmitter subsystem, coupled to said combiner, for transmitting the multichannel-spread-spectrum signal over a communications channel at a carrier frequency.

* * * * *

CERTIFICATE OF FILING AND SERVICE

I hereby certify that on April 1, 2016, I electronically filed the foregoing with the Clerk of the Court for the United States Court of Appeals for the Federal Circuit by using the appellate CM/ECF system.

I certify that all participants in the case are registered CM/ECF users and that service will be accomplished by the appellate CM/ECF system.

I further certify that, upon acceptance and request from the Court, the required paper copies of the foregoing will be shipped via overnight delivery to the Clerk, United States Court of Appeals for the Federal Circuit, 717 Madison Place, N.W., Washington, D.C. 20439.

Dated: April 1, 2016

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CERTIFICATE OF COMPLIANCE

Pursuant to Federal Rules of Appellate Procedure 28.1(e)(3) and 32(a)(7)(C), the undersigned hereby certifies that this brief complies with the type-volume limitation of Federal Rule of Appellate Procedure 28.1(e)(2)(B)(i).

1. This brief complies with the type-volume limitation of Fed. R. App. P. 32(a)(7)(B) and Federal Circuit Rule 32(b) because this brief contains 2,736 words, excluding the parts of the brief exempted by Federal Circuit Rule 32(b)(1)-(3).

2. This brief complies with the typeface requirements of Fed. R. App. P. 32(a)(5) and the type style requirements of Fed. R. App. P. 32(a)(6) because this brief has been prepared in a proportionally spaced typeface using Microsoft Word in 14-point Times New Roman Font.

Dated: April 1, 2016

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